FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER **10191/1466**

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/581663

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED:
PCT/DE99/03018	**(22.09.99) 22 September 1999**	**(15.10.98) 15 October 1998**

TITLE OF INVENTION
METHOD FOR PROCESSING SILICON BY ETCHING PROCESSES

APPLICANT(S) FOR DO/EO/US
BECKER, Volker; LAERMER, Franz; and SCHILP, Andrea

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau)
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unsigned).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report; and PCT/RO/101.

EXPRESS MAIL NO.: EL179952555US

U.S. APPLICATION NO. if known, see 37 C.F.R.1.5	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/581663	PCT/DE99/03018	10191/1466

17. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EUROPEAN PATENT OFFICE or JPO $840.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $670.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $750.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	31 - 20 =	0	X $18.00	$198.00	
Independent Claims	1 - 3 =	0	X $78.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1038.00	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$1038.00	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 1038.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$1038.00	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **$1038.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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R L Mayer
SIGNATURE

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NAME

June 15, 2000
DATE

EXPRESS MAIL CERTIFICATE

"EXPRESS MAIL" MAILING LABEL NUMBER EL179932333US

DATE OF DEPOSIT June 13, 2000

TYPE OF DOCUMENT National Phase Application

SERIAL NO. Awaited FILING DATE Herewith

I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE, BY BEING HANDED TO A POSTAL CLERK OR BY BEING PLACED IN THE EXPRESS MAIL BOX BEFORE THE POSTED DATE OF THE LAST PICK UP, AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

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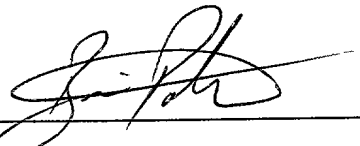

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[10191/1466]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)	:	Volker BECKER et al.
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	METHOD FOR PROCESSING SILICON BY ETCHING PROCESSES
Examiner	:	To Be Assigned
Art Unit	:	To Be Assigned

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

SIR:

Kindly amend the above-identified application before examination as set forth below.

IN THE SPECIFICATION:

On page 2, after line 32, insert the heading:

--SUMMARY OF THE INVENTION-- .

On page 4, line 10, insert the heading:

--DETAILED DESCRIPTION OF THE INVENTION-- .

On page 5, line 12, change "Drawing" to --BRIEF DESCRIPTION OF THE DRAWINGS--.

IN THE CLAIMS:

On page 22,delete the first line "Patent Claims" and insert:

--WHAT IS CLAIMED IS:--.

Claim 13, line 1, delete "or 11".

Claim 14, line 1, delete "or 11".

Claim 19, line 1, delete "17 or 18,".

Claim 22, lines 1-2, change "at least one of the preceding claims" to --claim 1--.

Claim 30, lines1-2, change "at least one of Claims 26 through 29" to --Claim 26--.

Claim 31, lines 1-2, change "at least one of the preceding claims" to --Claim 26--.

IN THE ABSTRACT:

On page 28, delete the first line and insert:

--ABSTRACT OF THE DISCLOSURE--.

Remarks

This Preliminary Amendment to the U.S. national stage of PCT Application No. PCT/DE99/03018 conforms the specification to U.S. Patent and Trademark Office rules and does not add new matter to the application.

The underlying PCT Application No. PCT/DE99/03018 includes an International Search Report, dated February 21, 2000. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report is included herewith.

Applicants assert that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully submitted,

Dated: June 15, 2000

By: RL Mayer

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METHOD FOR PROCESSING SILICON BY ETCHING PROCESSES

Background Information

The invention is based on a method for etching a silicon layered body as set forth by the species defined in the main claim.

The German laid open print 195 37 814 A1 describes a method for producing silicon layer systems, with which surface micromechanical sensors can be produced. To that end, deposited first on a silicon substrate is a thermal oxide upon which a thin layer of highly doped polysilicon is applied for use as a buried printed circuit trace. Deposited then on the polysilicon layer is a further oxide layer, and upon that, for example, a thick epipolysilicon layer. Finally, an aluminum metallization is deposited on the surface and patterned. The sensor structures to be exposed are subsequently etched out, preferably with a fluorine-based silicon deep-etching method described in the German patent 42 41 045. The sensor element is laid bare with the aid of a sacrificial-layer etching, in which the oxide below the sensor regions is removed by media containing hydrofluoric acid using a vapor-etching method. Disadvantageous in this undercutting technique is that the oxide is removed not only under the sensor region to be exposed, but also above and partially even under the polysilicon printed circuit traces, so that there is the danger of shunts and leakage current. Protection of the oxide regions whose undercutting is to be prevented, for instance, by protective lacquers, is only possible with considerable expenditure, since vaporous hydrofluoric acid penetrates almost all practicable polymer protective layers very quickly, and moreover, can act very

corrosively.

The German patent 44 20 962 A1 describes a dry-etching method in silicon for producing sensor structures by a combination of anisotropic and isotropic plasma-etching techniques. A subsequent wet-etching step or etching in the vapor phase is not necessary in this case. All the process steps can be carried out in one single plasma-etching installation. To that end, first of all, the sensor structure is produced with vertical walls with the aid of the anisotropic deep-etching method described in DE 42 41 045. In this context, deposition steps in which a Teflon-like polymer is deposited on the side wall, and fluorine-based etching steps which are isotropic as such and are made locally anisotropic by propelling the side-wall polymer during the etching, alternate. The silicon substrate is subsequently isotropically etched with a fluorine-based etching step until the silicon structure for the sensor element is completely exposed. However, this method has two serious disadvantages. On one hand, because of the "microloading effect", narrow etched trenches are etched more slowly than wide etched trenches, which then also holds true for the speed of the subsequent lateral undercutting, i.e., the undercutting progresses more slowly for narrow trenches than for wide trenches. Secondly, the structures to be exposed are also attacked from their lower side or bottom. The result is that structures which are surrounded by wide trenches have less residual height than structures which are surrounded by narrow trenches, which frequently leads to unreproducible and unsatisfactory mechanical properties of the sensor elements produced.

The object of the present invention is to provide a method for etching silicon or silicon layers with which trenches, defined initially by an etching mask, can be

etched anisotropically in a silicon layer. In this context, the etching depth achieved in the trenches should not be dependent on the width of the trenches, but rather only on the etching time. The intention is also to permit a defined undercutting, particularly of free-standing structures surrounded by trenches, e.g., for producing sensor elements. In addition, the bottom of the free-standing structures should not be etched during the undercutting.

Advantages of the Invention

Compared to the related art, the method of the present invention having the characterizing features of the main claim has the advantage that defined undercuttings are possible which permit free-standing structures to be produced in a defined and reproducible manner, it being possible to execute all the micromechanical patterning steps in one etching chamber without having to remove the silicon body in between. There is no etch attack on the free-standing structures starting from their bottoms or the side walls. Also achieved is that all the structures have a defined height which is defined by the thickness of the silicon layer applied, regardless of microloading effects, trench widths and the degree of an isotropic undercutting.

Moreover, the method of the present invention prevents corrosion problems, e.g., due to hydrofluoric acid vapors, and electrical shunts caused by undercutting of printed circuit traces. Buried conducting layers can be completely surrounded by a sufficiently thick silicon-dioxide layer to protect them from undercuttings and etch attacks.

A further advantage of the method is that deep undercuttings can also be implemented, thus permitting

large distances between the structure and the silicon substrate layer. For example, in the case of a sensor, this reduces the danger of an unintentional impact of the sensor element on the layer located beneath it in the event of an overload, with subsequent irreversible adhesion to one another ("sticking"). The distance between the sensor element and the silicon layer can be selected to be so large that they never touch each other, even in the case of an overload.

The method of the present invention can be carried out very advantageously in existing silicon deep-etching installations according to DE 42 41 045, so that no additional investment costs arise. In this context, by switching off the ion acceleration toward the substrate during an etching step, silicon structures can also be etched isotropically using this initially anisotropic plasma dry-etching method, to thus achieve undercutting of the silicon structures to be laid bare.

Since the etching mask applied during the etching processes, e.g., in the form of a photoresist mask on the silicon layer, is first removed after all etching is completed, during the etching, aluminum contact areas on the surface of the silicon layer, for example, are completely protected from corrosion, which otherwise is frequently unavoidable when working with etchant gases containing fluorine. Thus, a system integration can also be achieved in a particularly advantageous manner, i.e., producing a sensor element with integrated circuit on one and the same chip. Moreover, the method of the present invention for producing sensor elements, for example, is completely compatible with method steps in IC integration technology.

Since the method of the present invention prevents undercutting of conducting layers and an uncontrolled

formation of etch pockets in the etched silicon layer, swimming of particles in these pockets, which otherwise can scarcely be removed again and which lead to mechanical and electrical faults in sensor elements, is already also forestalled from the standpoint of process engineering.

Further advantages and advantageous further developments of the invention come to light from the measures specified in the subclaims.

Drawing

Exemplary embodiments of the invention are explained in greater detail in the following description with reference to the drawing. Figure 1 shows schematically the structure of a silicon layered body with an etching mask; Figure 2 shows the silicon layered body according to Figure 1 with trenches, and Figure 3 shows the silicon layered body according to Figures 1 and 2 with an undercut starting from the exposed region of the trenches. Figure 4 shows the structure of a silicon layered body with a completely enclosed intermediate layer as sacrificial layer; Figure 5 shows the silicon layered body according to Figure 4 with etched trenches; Figure 6 shows the silicon layered body according to Figures 4 and 5, respectively, with an undercut that starts from the exposed region of the trenches and is bounded laterally and vertically by separating layers; and Figure 7 shows a variant of the structure of the silicon layered body corresponding to Figure 6, the separating layer being formed continuously with a thin, patterned conducting layer enclosed therein. Figures 8 through 11 illustrate another exemplary embodiment as a further development of the exemplary embodiment according to Figure 7, an undercut starting from an intermediate layer into the free-standing structures being

purposefully permitted by interrupting the separating layer.

Exemplary Embodiments

Figure 1 shows a silicon layered body having a silicon layer, which in the following is designated as further silicon layer 17, upon which a separating layer is applied that itself is made of a plurality of separating-layer sections 12, 14, 16. A first separating-layer section 12 is made of thermally oxidized silicon (so-called silicon dioxide). Located on this, region-wise, is a thin, optionally patterned conducting layer 13 of conductive, highly doped polysilicon, followed by a second separating-layer section 16 made of silicon dioxide which was produced from the vapor phase by a deposition of silanes. In the regions free of conducting layer 13, which, according to Figure 1, are occupied by a third separating-layer section 14, first and second separating-layer sections 12, 16 have been completely etched back up to further silicon layer 17, and third separating-layer section 14 has subsequently been grown with a thickness of merely 10 nm to 100 nm at the same location, and is made of silicon dioxide. Located above separating-layer sections 12, 14, 16 is a first silicon layer 15 made of epipolysilicon. The surface of first silicon layer 15 is metal-plated and patterned with an etching mask 10 to define lateral recesses 21.

Figure 2 elucidates the result of a first anisotropic plasma etching process, having alternating deposition and etching steps, which etches trenches 21' in the region of lateral recesses 21, a Teflon-like film 20 building up on the side walls of trenches 21'. Upon reaching separating-layer sections 12, 14, 16, the first etching process comes almost to a complete standstill, since it exhibits a very high selectivity for silicon compared to silicon

dioxide, and thus silicon dioxide is virtually not etched. The achieved depth of trenches 21' is thus defined in each case by the depth of buried separating-layer sections 12, 14, 16, i.e., the thickness of first silicon layer 15. Exposed regions 23 and 24, respectively, are located at the bottom of trenches 21'.

Figure 3 clarifies how, in a second, for example, anisotropic plasma etching process under strong ion bombardment, exposed regions 23 of thin, third separating-layer section 14 are broken through or removed. Since second separating-layer section 16 above conducting layer 13 in exposed regions 24 is considerably thicker than third separating-layer section 14, second layer section 16 is merely slightly thinned when separating-layer section 14 is broken through. Because of this, conducting layer 13 remains completely enclosed by separating-layer sections 12, 16. After thin, third separating-layer section 14 has been broken through in exposed region 23, a further, preferably isotropic etching of further silicon layer 17 is carried out to produce a cavity 31. In so doing, a free-standing structure 32 is undercut and produced having a bottom 30 which is made of the material of separating-layer section 14. This bottom 30, possibly together with a separating-layer remainder 25 of third separating-layer section 14, as well as with Teflon-like films 20, prevents an etch-back and a structural loss of free-standing structure 32.

In the following, further details of the individual method steps are explained by way of example, corresponding to their sequence.

First of all, a thick first separating-layer section 12 is deposited on further silicon layer 17. First separating-layer section 12 preferably contains silicon dioxide, another silicon oxide, silicon nitride, glass, a

ceramic or a mixture thereof, and is deposited using deposition processes generally known from semiconductor technology, and particularly by thermal oxidation according to the teaching of DE 195 37 814 A1. Further silicon layer 17 is a silicon wafer.

For example, the thickness of separating-layer section 12 is 2.5 µm. The deposited and optionally patterned, thin conducting layer 13 preferably contains conductive polysilicon which can be highly doped to improve the conductivity. A further oxide, preferably silicon dioxide, is thereupon deposited as separating-layer section 16 on this layer system. This deposition is carried out, for example, from the vapor phase using silanes according to the method known per se from DE 195 37 814 A1, and has a layer thickness of approximately 1.5 µm. Conducting layer 13 is preferably completely enclosed or buried.

In the region of third separating-layer section 14, in which a free-standing structure 32 is later to be produced by undercutting, the oxide located there is subsequently thinned to a thickness of approximately 10 nm to 100 nm. This can be effected by time-controlled etching back of separating-layer sections 12 and 16. In a further exemplary embodiment, separating-layer sections 12 and 16 are completely etched back in third separating-layer section 14 until further silicon layer 17 is reached, in order to subsequently regrow a desired thickness of third separating-layer section 14 of, for example, 10 nm to 100 nm. This growth of third separating-layer section 14 can be carried out either only in the previously etched-back regions, or else over the entire surface in the etched-back regions and on remaining second separating-layer section 16, since the thickness of grown third separating-layer section 14 is virtually negligible compared to the thickness of second

separating-layer section 16. In this method variant of the complete etch-back and subsequent growth, the thickness of third separating-layer section 14, which is preferably made of thermally grown silicon dioxide, is very exactly defined.

In the preferred embodiment, first separating-layer section 12 has a greater density than second separating-layer section 16. Furthermore, the thickness of second separating-layer section 16 should be considerably greater, particularly more than ten times to one thousand times greater, than the thickness of the etched-back separating-layer section or of grown third separating-layer section 14. The thickness of first and second separating-layer sections 12 and 16, respectively, in each case lies absolutely between 500 nm to 50 µm, preferably between 1 µm to 10 µm.

In the subsequent method step, a thick first silicon layer 15, preferably of epipolysilicon, is grown on separating-layer sections 12, 14, 16, is optionally plated on the surface and, for example, is patterned with etching mask 10 to define lateral recesses 21. First silicon layer 15 can also be doped. The plated surface of first silicon layer 15 can be an aluminum contact layer which is simultaneously protected from the attack of fluorine-containing gases by etching mask 10, e.g., in the form of a photoresist mask.

Thereupon, using an anisotropic deep-etching process known per se from DE 42 41 045 or DE 44 20 962 A1 as the first etching process, trenches 21' are etched at the locations of lateral recesses 21. Upon reaching separating-layer sections 12, 14, 16 in exposed regions 23 and 24, respectively, this first etching process comes virtually to a standstill, since the etching method known from DE 42 41 045, to which this exemplary embodiment

relates, exhibits a very high selectivity of approximately 200-300:1 with respect to silicon dioxide, which means that etching virtually stops on separating-layer sections 12, 14, 16 which are preferably made of silicon dioxide. In addition to the composition of the separating layer, the etching stop is determined in particular by the etching process selected. The method parameters should always be selected in such a way that etching virtually stops upon reaching separating-layer sections 12, 14, 16.

The preferred first etching process according to DE 42 41 045 is a dry etching process in which deposition steps are carried out alternating with isotropic etching steps as such, a deposition gas, preferably octafluorocyclobutane C_4F_8 or perfluoropropylene C_3F_6, supplying polymer-forming monomers being exposed during the deposition steps to a highly dense plasma, particularly a PIE plasma (propagation ion etching) or an ICP plasma (inductively coupled plasma) which builds up Teflon-like film 20 of $(CF_2)_n$ on the side walls of trenches 21'; and in which method, an etchant gas, in particular sulfur hexafluoride SF_6, supplying fluorine radicals is used during the etching processes, to which oxygen can be admixed for suppressing a sulfur deposition in the waste-gas zone. By propelling Teflon-like side-wall film 20 during the etching steps which are isotropic as such, these steps become locally anisotropic.

In a second etching process, separating-layer sections 12, 14, 16 are now further etched in exposed regions 23 and 24, respectively, with an etching process suitable for etching the composition of the separating layer. This further etching is carried on until separating-layer section 14 is completely etched through in exposed regions 23. This is preferably done by a plasma etching method with an etching device according to the teaching

of DE 42 41 045, using etchant gases CF_4, C_2F_6, C_3F_8, CHF_3, C_3F_6 or C_4F_8, with application of strong ion bombardment, i.e., high substrate bias voltage. Particularly when using fluorine-rich etchant gases CF_4, C_2F_6, C_3F_8, or a mixture of CF_4 and CHF_3, this oxide etching process is unproblematic for the state of the plasma etching chamber with respect to subsequent silicon etchings. If, for example, for reasons of higher selectivity, the intention is to use fluorine-poorer oxide etchant gases CHF_3, C_3F_6 or C_4F_8, the process parameters must be optimized very carefully to prevent later silicon etchings in the chamber from being poisoned by cross-contamination. However, it is also possible to carry out the oxide etching in an etching installation especially provided for this purpose. To this end, a cluster installation is used in particular, in which a single handling system serves a plurality of plasma etching chambers and in which the silicon body always remains in vacuum.

In further method variants, the oxide etching of exposed regions 23 and 24, respectively, of separating-layer sections 12, 14, 16 can also be carried out using a wet chemical treatment, in that the layer sequence, produced, for example, on a wafer, is removed from the plasma etching chamber and a silicon dioxide layer in exposed regions 23 and 24, respectively, is then etched with diluted hydrofluoric acid or a sufficiently buffered hydrofluoric acid solution, and is completely removed in exposed regions 23. However, the preferred embodiment of the invention is the etching using a dry chemical treatment with the aid of a plasma, since this method in particular does not undercut the oxide edges of bottom 30 or of separating-layer remainders 25.

When etching through third separating-layer section 14 in exposed regions 23, the separating-layer sections in exposed region 24 of second separating-layer section 16

are unavoidably partially removed as well, since this second etching process is carried out unmasked and therefore over the entire surface on all exposed regions 23 and 24, respectively. However, since second separating-layer section 16 has a considerably greater thickness of, for example, 1.5 µm compared to only approximately 50 nm of third separating-layer section 14, this etching of second separating-layer section 16 when etching through the exposed regions of thin, third separating-layer section 14 is of no importance, even given a double overetching for reasons of process reliability when etching through. Therefore, buried conducting layer 13, in particular, remains protected all over by a thick, intact silicon dioxide layer.

After third separating-layer section 14 has been etched through in exposed regions 23, according to Figure 3, an isotropic etching of further silicon layer 17 is carried out in a third etching process. Prior to this etching, an additional passivation of the side walls of trenches 21' with a Teflon-like plasma polymer can be carried out according to the teaching of DE 44 20 962 A1, provided that this side-wall passivation did not already come about during the etching of trenches 21' according to Figure 2 and been retained complete and undamaged when etching through third separating-layer section 14 in exposed regions 23. The isotropic etching of further silicon layer 17 is preferably an undercutting in region 31, which results in laying bare structure 32 to be exposed. No etching of bottom 30 or of the side walls of free-standing structure 32 can occur during this etching of further silicon layer 17, since bottom 30 is protected, for example, by a thin silicon dioxide layer from third separating-layer section 14, and the side walls are protected by Teflon-like film 20. The same holds true for an etch-back into first silicon layer 15, or an etch-back into conducting layer 13, which are

likewise protected by separating-layer remainders 25 not etched through in the second etching process.

Specifically, the third etching process for the isotropic etching of further silicon layer 17 is carried out by initially removing remainders of a fluoropolymer possibly still present on further silicon layer 17 after etching through third separating-layer section 14. This is done by letting argon and/or oxygen into the etching chamber for a short time and igniting the plasma again. In so doing, polymer is very quickly removed selectively on the etching ground by ion action in a generally known manner, resulting in a polymer-free further silicon layer 17 and a side-wall passivation by Teflon-like films 20 which continues to be intact. The presence of oxygen promotes this physical etching removal by directed ions, in that chemical reactions are induced between fluorocarbons and oxygen. Thereupon, an isotropic silicon etching method with a fluorine plasma is carried out in a manner known per se according to DE 42 41 045, an SF_6 plasma being ignited in an inductive plasma source, and at the same time, the side-wall film transport mechanism known from DE 42 41 045 being forestalled by using a high process pressure and applying no substrate bias voltage. A suitable gas flow for this part of the third etching process is, for example, 100 sccm SF_6 at a pressure of 50 to 100 mTorr. In a variant of this etching process, the initial removal of the remainders of a fluoropolymer on further silicon layer 17 can also be carried out in the manner that the silicon etching method according to DE 42 41 045 with a fluorine plasma and the indicated parameters is started for a few seconds with a high substrate bias power of 50 to 100 W, and this substrate bias power is then completely switched off. With these means, the remainders of the fluoropolymer on further silicon layer 17 are removed within the few seconds, while Teflon-like side-wall films 20 remain essentially

unchanged.

Alternatively, the isotropic fluorine etching step in the third etching process for the isotropic etching of further silicon layer 17 after the removal of the remainders of the fluoropolymer on further silicon layer 17 can be carried out without plasma support, using etchant gases such as xenon difluoride, chlorotrifluoride, bromine trifluoride or iodine pentafluoride which, as is known, immediately attack free silicon areas isotropically in vigorous reaction, forming volatile silicon tetrafluoride. The selectivity of these gases with respect to non-silicon is extremely high, so that the thinnest passivation layers are already sufficient for protecting from etch attacks.

Since in the isotropic undercutting, the silicon dioxide remains at bottom 30 of structure 32 to be exposed, third separating-layer section 14 must be as thin as possible so as not to disadvantageously influence the mechanical properties of free-standing structure 32 which, for example, can be used as a sensor element. A practicable lower limit of the thickness is approximately 10 nm. In addition, due to the silicon-dioxide layer at bottom 30 of free-standing structure 32, a compressive strain is induced which causes a slight curvature of bottom 30 upward. Given a layer thickness of approximately 10 nm, this curvature is negligible in most cases. However, it is also possible to completely compensate for this compressive strain by a doping of first silicon layer 15 from above.

Due to the method of the present invention, free-standing structures 32 have a height, in particular, which is determined only by the thickness of first silicon layer 15, and is independent of microloading effects, the degree of isotropic etching and undercutting,

respectively, and the trench widths.

After removal from the plasma etching installation, etching mask 10, e.g., in the form of a photoresist mask, and the remaining passivating Teflon-like films 20 are removed from the etched silicon body in an oxygen plasma stripper with the aid of an oxygen plasma ashing process known in semiconductor technology. Thus, not until this stage are the plated surface of first silicon layer 15 and aluminum contact areas optionally applied there, which previously were lying under etching mask 10 from corrosion and etch attacks, also laid bare. Therefore, any aftertreatment of these contact areas can be eliminated. This method is particularly suited for producing sensor elements having free-standing structures, in which the associated integrated circuit is arranged on the same wafer.

Since Teflon-like films 20 represent an excellent means for preventing irreversible bonding of micromechanical structures upon contact of silicon with silicon ("sticking"), for many applications it is advisable for these Teflon-like films 20, which are also removed when removing etching mask 10 in an oxygen ashing process, to be applied again later by a fresh Teflon coating. This can already be done in the oxygen plasma stripper by, in conclusion, instead of oxygen, letting in for a short time a gas such as C_3F_6, C_4F_8 or CHF_3 supplying Teflon-forming monomers, and igniting the plasma again. Because of this, however, an aluminum plating on the surface of silicon layer 15 is also covered with Teflon, which can cause problems during a later contacting. Therefore, in a particularly advantageous refinement of the invention, after the oxygen ashing process, Teflon-like films 20 are again applied over the entire surface on all accessible silicon areas with the deposition step already known from DE 42 41 045 in the etching reactor, and subsequently

removed again with the aid of a short-duration, strong ion bombardment on all areas accessible for the normal ionic incidence, so that Teflon-like films 20 are retained only on the side walls of free-standing structure 32, bottom 30 and all silicon- or silicon-oxide areas shadowed from the ionic incidence. Consequently, contact areas, in particular, are freed again from an unwanted Teflon coating. Alternatively, instead of later removing the Teflon-like films on all locations accessible for the normal ionic incidence, it can also be very advantageous to use an ionic bombardment already during the application of the Teflon-like films according to DE 42 41 045 in the etching reactor, so that in particular, the Teflon-like films really do not form at all on the contact areas (selective coating of the side walls).

As a further exemplary embodiment, Figures 4, 5 and 6 show a variant of the exemplary embodiment described with the aid of Figures 1 through 3, this exemplary embodiment differing from that one in that, before growing first silicon layer 15, initially an intermediate layer is additionally applied as a further silicon layer on third separating-layer section 14 using generally known deposition and patterning methods, and is subsequently surrounded on the surface and sides by a further separating layer 14'. Intermediate layer 17', used as a sacrificial layer, can be patterned according to the geometry needed. In this variant, third separating-layer section 14 can correspond very advantageously to first separating-layer section 12 with respect to thickness and composition, since further separating layer 14' now assumes the role of third separating-layer section 14 from the exemplary embodiment according to Figures 1 through 3. Consequently, further separating layer 14' is made, in particular, of thermally grown silicon dioxide having a thickness of 10 nm to 100 nm. In this respect,

an etch-back of third separating-layer section 14, or a growth of third separating-layer section 14 after a complete etch-back up to further silicon layer 17, as explained in the exemplary embodiment according to Figures 1 through 3, is no longer necessary, since not the third separating-layer section 14, but rather further separating layer 14' is etched through in the second etching process, and the third etching process therefore causes etching of intermediate layer 17' as the further silicon layer. Particularly advantageously, intermediate layer 17' can now also be patterned out from conducting layer 13 which is made of polysilicon, so that an additional process step for growing intermediate layer 17' is eliminated.

For example, intermediate layer 17', used as the sacrificial layer, has a composition like further silicon layer 17. It can also be made of polysilicon or epipolysilicon in accordance with conducting layer 13 or first silicon layer 15. Therefore, corresponding to the preceding exemplary embodiment, the first etching process stops in exposed regions 23' on further separating layer 14', as well as on exposed regions 24. In the second etching process, according to Figures 5 and 6, this thin further separating layer 14' is then again broken through in exposed regions 23' in an anisotropic plasma etching process corresponding to the preceding exemplary embodiment, under strong ion bombardment. Finally, as shown in Figure 6, using a third etching process corresponding to the preceding exemplary embodiment, a further isotropic etching of intermediate layer 17', used as the sacrificial layer, is then carried out, which in the exemplary embodiment according to Figure 3, would correspond to the isotropic etching of further silicon layer 17 for producing cavity 31. Because intermediate layer 17' in this exemplary embodiment is initially completely enclosed by separating layer 14' and third

separating-layer section 14, respectively, in the third etching process, the etching stops automatically after intermediate layer 17', used as the sacrificial layer, is completely etched away, so that on one hand, a free-standing structure 32 having defined bottom 30 and defined side walls is formed, and on the other hand, a cavity 31' is formed having edges 33 that are exactly defined laterally and vertically on the basis of the patterning, i.e., the geometry and thickness of further separating layer 14'.

According to a further exemplary embodiment, which otherwise is largely analogous to the exemplary embodiment according to Figures 4, 5 and 6, and which is explained with the aid of Figure 7, separating layer 12, 14, 16 is formed continuously with uniform thickness on further silicon layer 17, and optionally-patterned conducting layer 13 is enclosed therein. Analogous to Figure 4 and the preceding exemplary embodiment, the intermediate layer is then additionally applied as further silicon layer on this separating layer 12, 14, 16 using generally known deposition and patterning methods, and is subsequently surrounded on the surface and sides by further separating layer 14' which, for example, is produced by thermal growth of a silicon dioxide layer. The composition of this further separating layer 14' and its thickness in turn preferably correspond to that of third separating-layer section 14. Intermediate layer 17' is composed, in particular, like further silicon layer 17, conducting layer 13 or first silicon layer 15.

Thus, this variant of the method according to the invention makes it possible to place electrode areas under active or free-standing structures, an optionally patterned plane with intermediate layer 17' as sacrificial layer being freely available which is removed for producing free-standing structures 32, as well as a

plane, located under it, having electrode and printed-circuit-trace geometries which are protected, in particular, from etch attacks by separating-layer sections 12, 14, 16. Therefore, patternings can be carried out independently of one another in both planes. Furthermore, after the removal of intermediate layer 17', all electrically functional, patterned conducting layers 13 are still present, completely electrically insulated to all sides.

A further advantageous development of the invention is illustrated as exemplary embodiment on the basis of Figures 8 through 11, the various etching processes, layer compositions and layer thicknesses being selected as already explained in the preceding exemplary embodiments. However, in further development of Figure 7 (see Figure 8), this example provides that, due to a suitable, generally known patterning of further separating layer 14', said further separating layer 14' and third separating-layer section 14 do not completely enclose intermediate layer 17'.

The layered structure of the layered body shown is implemented in detail as already described in the preceding exemplary embodiments. Thereupon, as shown in Figure 9, trenches 21' are produced in a first etching process, accompanied by simultaneous buildup of the side-wall passivation by Teflon-like films 20, the first etching process coming to a standstill at bottom 23' of trenches 21'. In the second etching process, thin, further separating layer 14' is then broken through at bottom 23' of trenches 21'. In so doing, third separating-layer section 14 is also simultaneously etched at bottom 23 at the locations at which a further separating layer 14' lying above is missing. However, in view of the slight thickness of further separating layer 14' and of second separating-layer section 16 present

below third separating-layer section 14, this etching is negligible.

In this exemplary embodiment, in an advantageous further development of the invention, it is possible in particular to completely dispense with third separating-layer section 14, since its task is assumed by further separating layer 14' and by second separating-layer section 16. After breaking through further separating layer 14' at bottom 23' of trenches 21', the second etching process is interrupted. Following is the third etching process, already previously described, which etches intermediate layer 17' used as the sacrificial layer. In this context, the etch attack in the third etching process is restricted to the region bounded by thin, further separating layer 14' and third separating-layer section 14 or second separating-layer section 16; in this exemplary embodiment, however, differing from Figure 7, the patterning of further separating layer 14' also makes it possible to very advantageously carry out an etching coming from below within a rib 40. In so doing, the advance of the etching front in rib 40 is restricted by the side-wall passivation due to the Teflon-like films 20 and by the upper passivation of ribs 40 by etching mask 10, so that rib 40 is largely hollowed out or interrupted locally as the etching progresses. Consequently, by selective omission or a defined patterning of further separating layer 14', this exemplary embodiment of the invention selectively permits an etch attack from below in the third etching process. Therefore, as shown in Figure 11, for example, an initially produced silicon bridge can be selectively cut through from below by an etch attack under an aluminum plating, present on the surface in the first silicon layer 15 and constructed in the form of dielectrically insulated printed circuit traces. Thus, a free printed circuit trace is obtained, at least locally, which is

available for further contacting, as well as an electrical isolation of free-standing structure 32 from the surrounding silicon. Therefore, this exemplary embodiment offers new possibilities and advantages, particularly from the standpoint of integration, i.e., the use of micromechanics with electronic circuit technology.

Particularly when the surface aluminum plating is separated from actual first silicon layer 15 by an additional, suitably patterned, electrically insulating intermediate layer made, for example, of silicon dioxide - this intermediate layer not being etched during the third etching process - it is possible to selectively achieve an electrical connection and, in particular, an interface connection of a sensor to an electronic evaluation circuit via a surface plating of first silicon layer 15, which is stretched like a bridge over an abyss and is protected from below by the electrically insulating intermediate layer not etched in the third etching process.

Patent Claims

1. A method for etching a silicon layered body having a first silicon layer (15) which is provided with an etching mask (10) for defining lateral recesses (21), work being carried out in a first etching process with a plasma, and trenches (21') being formed by anisotropic etching in the region of the lateral recesses (21), characterized in that, buried between the first silicon layer (15) and a further silicon layer (17, 17') is at least one separating layer (12, 14, 14', 16), upon reaching which, the first etching process comes at least almost to a standstill; that the separating layer (12, 14, 14', 16) is thereupon etched through in an exposed region (23, 23') by a second etching process; and that a third etching process subsequently etches the further silicon layer (17, 17').

2. The method as recited in Claim 1, characterized in that a complete isotropic undercutting is produced between at least two trenches (21') by the third etching process in such a way that a free-standing structure (32) is formed.

3. The method as recited in Claim 1, characterized in that the first etching process is a dry etching process in which deposition steps are carried out alternating with generally known isotropic etching steps, a deposition gas, preferably octafluorocyclobutane C_4F_8 or perfluoropropylene C_3F_6, supplying polymer-forming monomers being exposed during the deposition steps to a highly dense plasma, particularly a PIE plasma (propagation ion etching) or an ICP plasma (inductively coupled plasma) which builds up a Teflon-like film 20 of $(CF_2)_n$ on the side walls of the trenches (21'); and in that an etchant gas, in particular sulfur hexafluoride SF_6 supplying fluorine radicals, with admixed oxygen, is used

during the etching processes.

4. The method as recited in Claim 1,
characterized in that the first, anisotropic etching process of the trenches (21') exhibits a high selectivity with respect to silicon dioxide.

5. The method as recited in Claim 1,
characterized in that the separating layer (12, 14, 14', 16) is formed from at least a first separating-layer section (12) and a second separating-layer section (16), the first separating-layer section (12) containing silicon dioxide, another silicon oxide, silicon nitride, glass, a ceramic or a mixture thereof, and being deposited using deposition methods known from semiconductor technology, and the second separating-layer section (16) preferably being a silicon dioxide layer.

6. The method as recited in Claim 1,
characterized in that the second etching process for etching through the separating layer (12, 14, 14', 16) in the exposed region (23, 23') of the trenches (21') is carried out using a dry chemical treatment, preferably with the aid of plasma etching.

7. The method as recited in Claim 6,
characterized in that the plasma etching is carried out under strong ion bombardment and with the aid of an etchant gas, preferably CF_4, C_2F_6, C_3F_8, CHF_3, C_3F_6 or C_4F_8.

8. The method as recited in Claim 1,
characterized in that the second etching process for etching through the separating layer (12, 14, 14', 16) in the exposed region (23, 23') of the trenches (21') is carried out with a wet chemical treatment, and particularly with the aid of diluted hydrofluoric acid or hydrofluoric acid solutions.

9. The method as recited in Claim 1,
characterized in that the exposed structures (32) have a bottom (30) which is at least largely free of an etch attack during etching, particularly during the undercutting in the third etching process.

10. The method as recited in Claim 1,
characterized in that, prior to or during the third etching process, the side walls of the trenches (21'), prior to the undercutting, are selectively coated with a plasma polymer for producing a Teflon-like film (20).

11. The method as recited in Claim 5,
characterized in that, applied on the further silicon layer (17) is the first separating-layer section (12), upon which a conducting layer (13) is then deposited, at least region-wise, and optionally patterned, the conducting layer being made preferably of conductive, highly doped polysilicon; and that the second separating-layer section (16) is thereupon deposited onto the conducting layer (13).

12. The method as recited in Claim 11,
characterized in that the first and second separating-layer sections (12, 16) are deposited in such a way that the conducting layer (13) is completely enclosed.

13. The method as recited in Claim 5 or 11,
characterized in that the second separating-layer section (16) is deposited from the vapor phase, in particular by decomposition of silanes.

14. The method as recited in Claim 5 or 11,
characterized in that the first separating-layer section (12) is formed from thermally grown silicon dioxide.

15. The method as recited in Claim 5,

characterized in that the separating-layer sections (12) and (16) each have a thickness of 500 nm to 50 µm, in particular of 1 µm to 10 µm.

16. The method as recited in Claim 5,
characterized in that the first and/or the second separating-layer section (12, 16) in the vicinity of at least one trench (21') or an exposed structure (32) are thinned by etching back to an etched-back separating-layer section having a thickness of 10 nm to 100 nm, or are completely removed and, instead, a third separating-layer section (14) of less thickness is subsequently grown, preferably from silicon dioxide.

17. The method as recited in Claim 16,
characterized in that the third separating-layer section (14) is produced with a thickness of 10 nm to 100 nm.

18. The method as recited in Claim 16,
characterized in that the first silicon layer (15) is grown on the second separating-layer section (16) and the etched-back separating-layer section, or on the separating-layer section (16) and the grown, third separating-layer section (14).

19. The method as recited in Claim 16, 17 or 18,
characterized in that the second separating-layer section (16) is thicker, in particular more than ten times to one thousand times thicker, than the etched-back separating-layer section or the third separating-layer section (14).
20. The method as recited in Claim 1,
characterized in that the first silicon layer (15) is made of epipolysilicon which is optionally doped and/or plated on the surface and/or patterned.

21. The method as recited in Claim 20,
characterized in that the plated surface of the first

silicon layer (15) is an aluminum contact layer which is protected from the attack of fluorine-containing gases by a photoresist mask as etching mask (10).

22. The method as recited in at least one of the preceding claims,
characterized in that the depth of the trenches (21') etched in the first etching process is independent of the ratio of width to height of the trenches (21'), and is set on the basis of the etching time for achieving the exposed regions (23, 23') of the first separating-layer section (16), of the grown, third separating-layer section (14) or of the further separating layer (14').

23. The method as recited in Claim 1,
characterized in that all the etching processes are carried out in a single etching chamber, and that in particular, the silicon layered body remains in the etching chamber during the etching processes.

24. The method as recited in Claim 1,
characterized in that the etching mask (10) and the remaining Teflon-like films (20) are finally removed from the etched silicon layered body in an oxygen plasma stripper by an oxygen ashing process.

25. The method as recited in Claim 24,
characterized in that, after the removal of the remaining Teflon-like films, a Teflon-like coating is applied on the side walls of the free-standing structure (32), the side walls of the trenches (21') and all areas shadowed from the normal ionic incidence, in the course of which, electrical contact areas, in particular, remain free from a Teflon-like coating.

26. The method as recited in Claim 18,
characterized in that, prior to growing the first silicon

layer (15) on the grown third separating-layer section (14) or the etched-back separating-layer section, first of all an intermediate layer (17'), which forms the further silicon layer as sacrificial layer, is applied, and that this intermediate layer (17') is subsequently covered with a further separating layer (14'), at least in the exposed regions (23, 23').

27. The method as recited in Claim 26,
characterized in that the intermediate layer (17') is grown from silicon, epipolysilicon, polysilicon, or conductive and/or doped polysilicon.

28. The method as recited in Claim 26,
characterized in that the further separating layer (14') is produced from thermally grown silicon dioxide.

29. The method as recited in Claim 28,
characterized in that the further separating layer (14') has a thickness of 10 nm to 100 nm.

30. The method as recited in at least one of Claims 26 through 29,
characterized in that, due to a patterning of the further separating layer (14'), the intermediate layer (17') is not completely surrounded by the further separating layer (14') and by a separating-layer section (14, 16).

31. The method as recited in at least one of the preceding claims for producing sensor elements having free-standing structures (32).

Abstract

A method is proposed for etching a first silicon layer (15) that is provided with an etching mask (10) for defining lateral recesses (21). In a first plasma etching process, trenches (21') are produced in the region of the lateral recesses (21) by anisotropic etching. The first etching process comes virtually to a standstill as soon as a separating layer (12, 14, 14', 16), buried between the first silicon layer (15) and a further silicon layer (17), is reached. This separating layer is thereupon etched through in exposed regions (23, 23') by a second etching process. A subsequent third etching process then etches the further silicon layer (17, 17'). In this manner, free-standing structures for sensor elements can be produced in a simple process which is completely compatible with the method steps in IC integration technology.

Figure 6

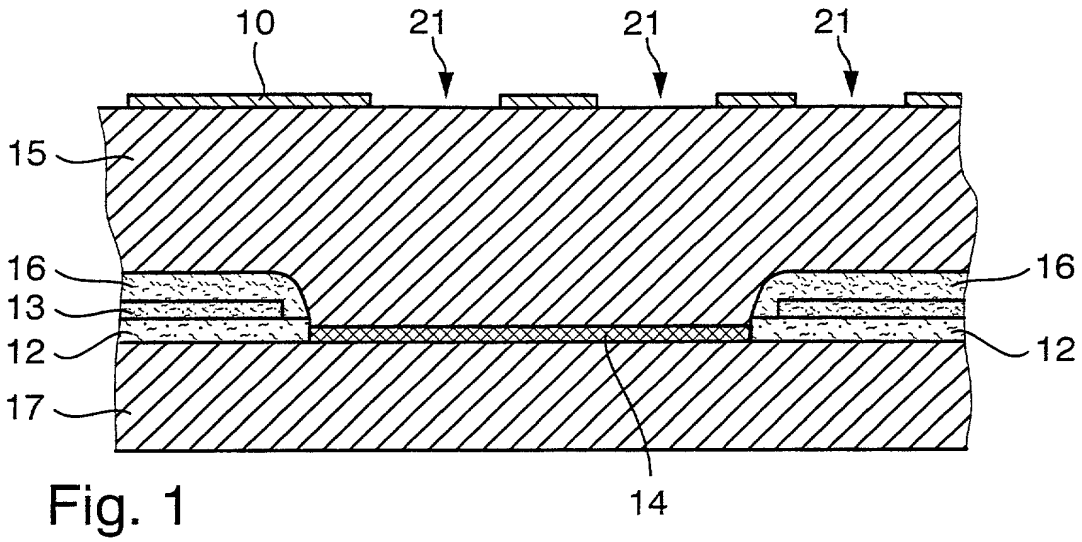


Fig. 1

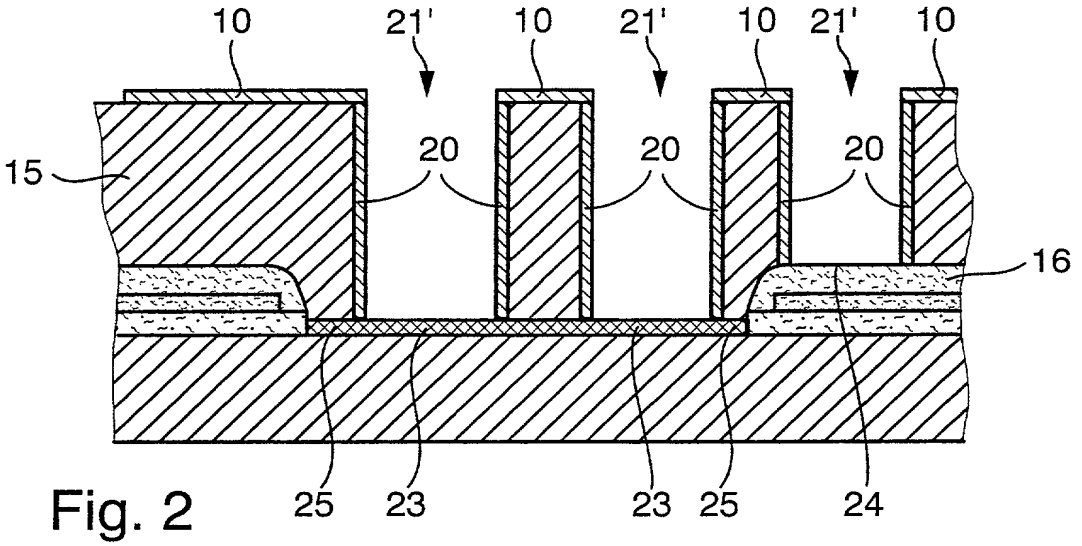


Fig. 2

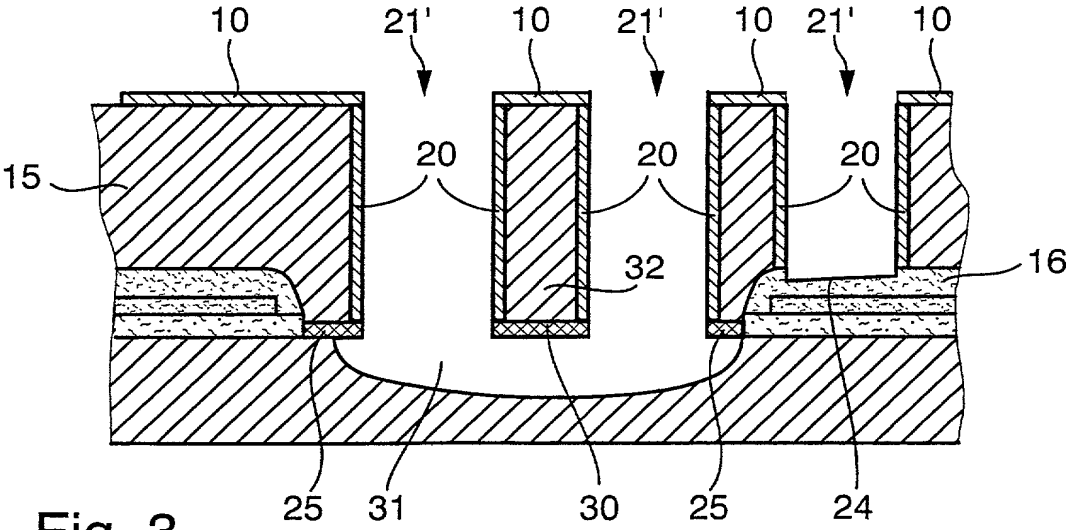


Fig. 3

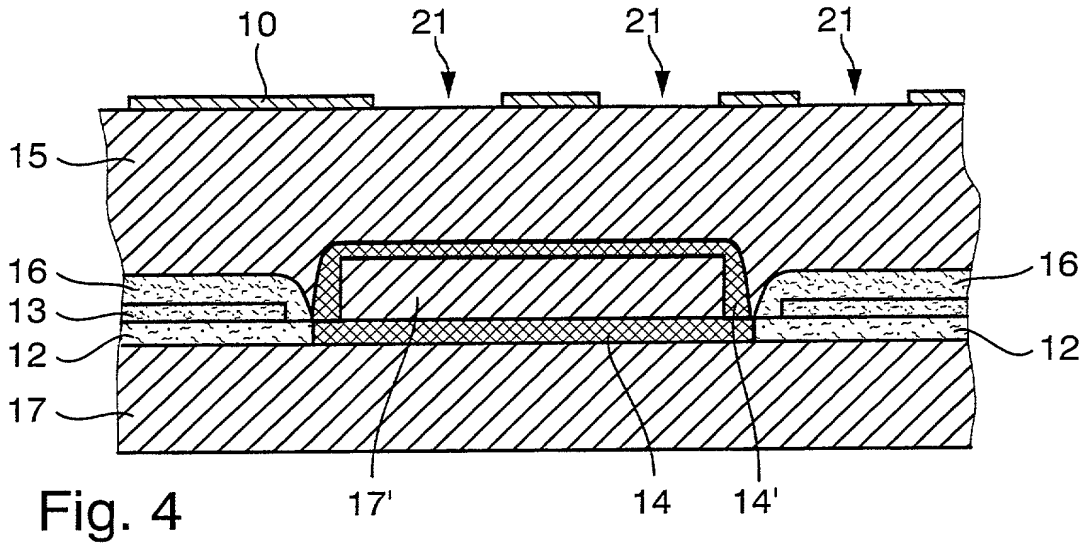


Fig. 4

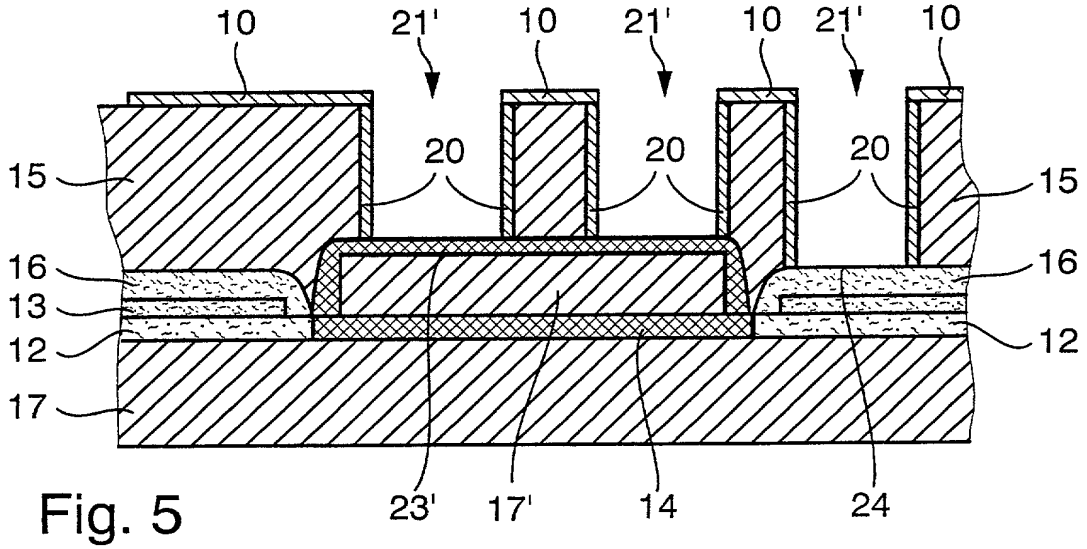


Fig. 5

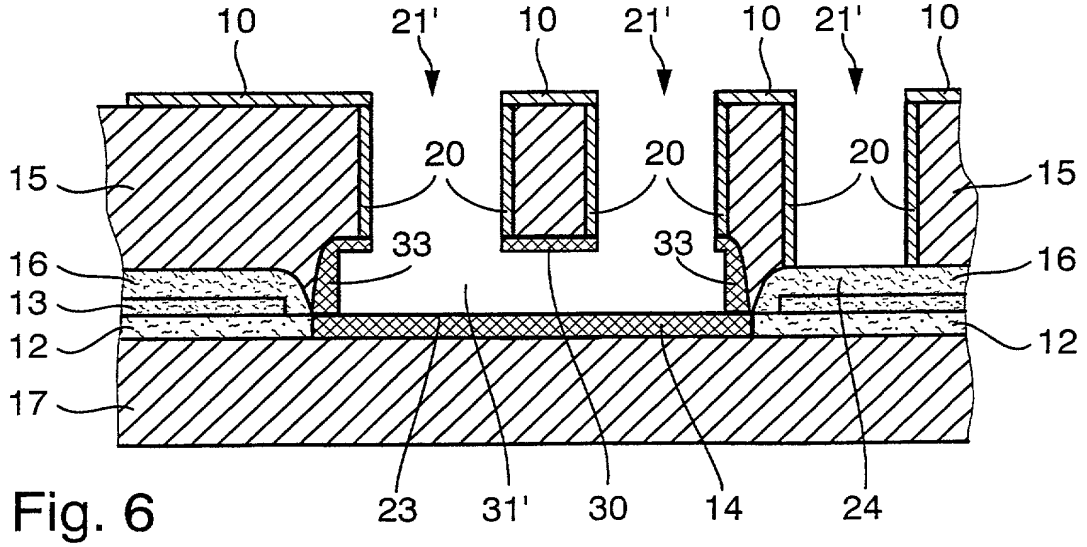
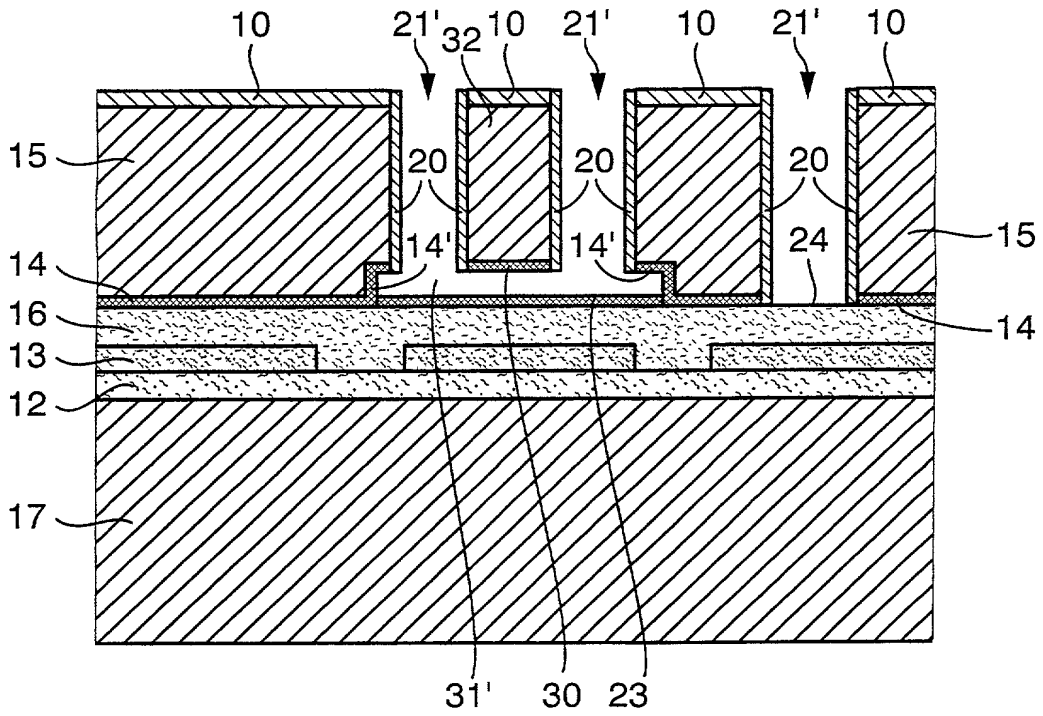


Fig. 6


10
21'
32
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21'
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21'
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15
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14
16
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13
12
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31'
30
23

Fig. 7

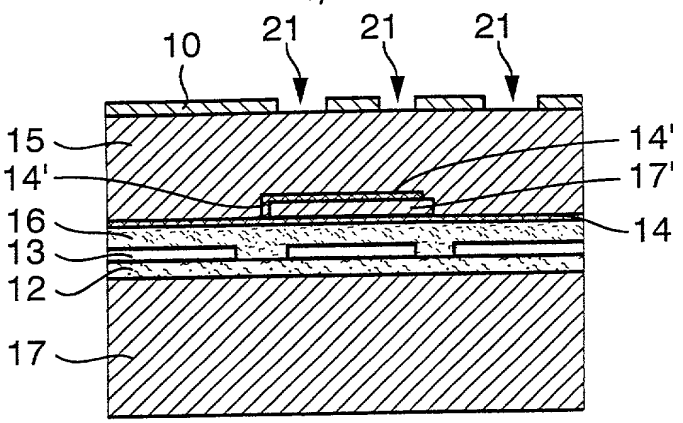

Fig. 8

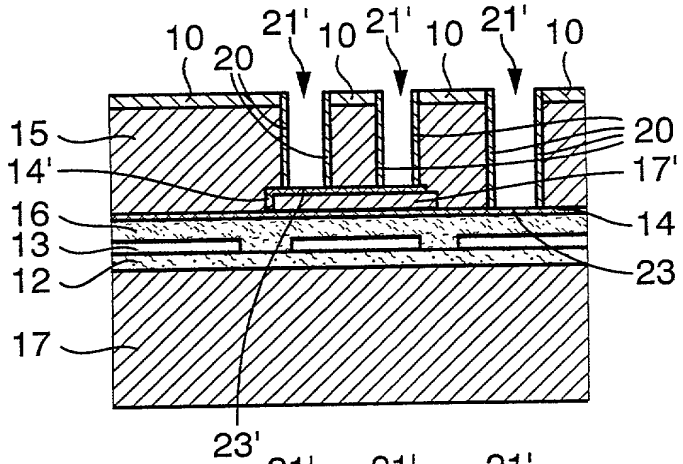

Fig. 9

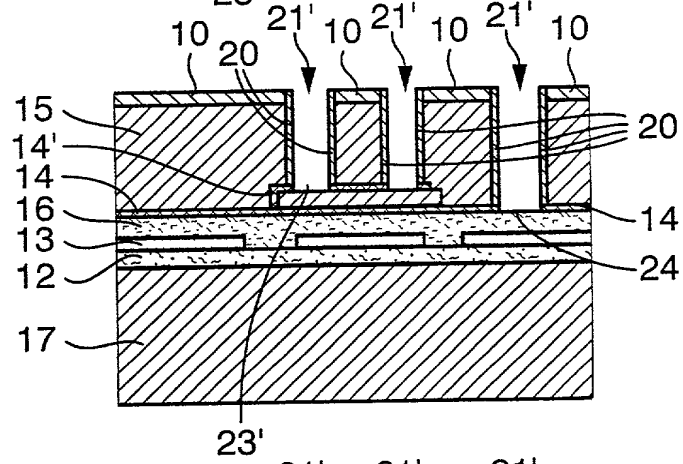

Fig. 10

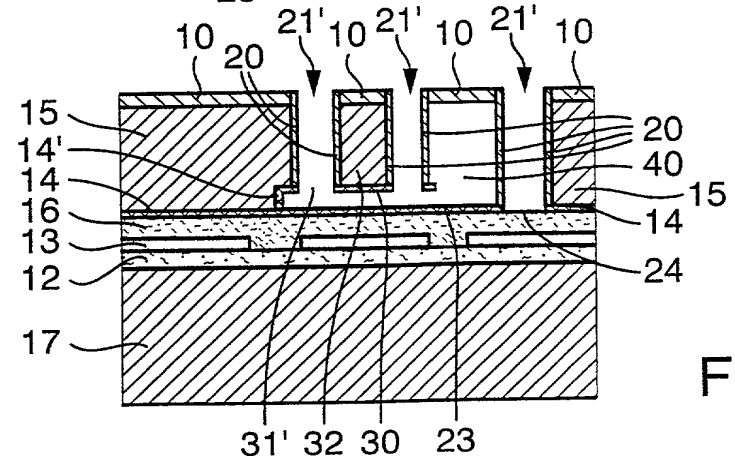

Fig. 11

[10191/1466]

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD FOR PROCESSING SILICON BY ETCHING PROCESSES**, for which an application for Letters Patent was filed as PCT International Application Number **PCT/DE99/03018** on September 22, 1999.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Number	Country	Day/month/year filed	Priority Claimed Under 35 USC § 119
198 47 455.5	Germany	15 October 1998	Yes

And I hereby appoint Richard L. Mayer (Reg. No. 22,490) and Gerard A. Messina (Reg. No. 35,952) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Exp. Mail No. EL179952755US

Please address all communications regarding this application to:

KENYON & KENYON
One Broadway
New York, New York 10004

Please direct all telephone calls to Richard L. Mayer at (212) 425-7200.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful and false statements may jeopardize the validity of the application or any patent issued thereon.

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witnessed by: Franz Lärmer
Franz Lärmer

Inventor: **Franz LAERMER**

Inventor's Signature: Franz Laermer

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witnessed by: Volker Becker

Volker Becker

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witnessed by: Franz Lövner
Franz Lövner